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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,592	11/27/2001	Raghavan Menon	VIVC001/00US	9102
5514 7590 05/22/2007 FITZPATRICK CELLA HARPER & SCINTO 30 ROCKEFELLER PLAZA NEW YORK, NY 10112			EXAMINER JONES, PRENELL P	
			ART UNIT	PAPER NUMBER
			2616	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No. 09/994,592	Applicant(s) MENON ET AL.	
	Examiner Prenell P. Jones	Art Unit 2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 05 March 2007.
- 2a) This action is **FINAL**.
- 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-50 and 53-104 is/are pending in the application.
 - 4a) Of the above claim(s) 33-36 and 98-104 is/are withdrawn from consideration.
- 5) Claim(s) 1-32, 37-40, 42-50 and 53-97 is/are allowed.
- 6) Claim(s) 41 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 - Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 - Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 - 1. Certified copies of the priority documents have been received.
 - 2. Certified copies of the priority documents have been received in Application No. _____.
 - 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) Notice of Informal Patent Application
- 6) Other: _____

Response to Arguments

1. Applicant's arguments with respect to claims 1-50 and 53-104 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues with respect to claim 41, that the cited art fails to teach "cells substantially aligned in time within a timeout period.

Examiner has used the same prior art, however, the rejection has been re-worded to clarify Examiner's intentions.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Surazski et al (US Pat 6,657,983) in view of Bonomi et al (US Pat 6,219,352).

Regarding claim 41, Surazski et al (US Pat 6,657,983) discloses scheduling and managing routing of ATM data in a communication system, wherein the architecture includes plurality of cells that make up a frame/packet accompanied by mini-slots (timeslots) time received/arrival time, and burst of packets or synchronous (substantially aligned in time) data stream (plurality of cells) are received (every cell/burst) in a specific scheduling period wherein the scheduling period is a time interval (timeout period) in which cells arrive (col. 8, line 21-67), and received burst packet is transmitted with timeslot and timestamp in a specified scheduling period, output cells associated with burst packet are coupled to a frame module/framer for further cell processing (Abstract, Figs. 9, 11, 12, col. 2, line 56-67, col. 4, line 12-30, col. 5, line 23-45, line 54-67, col. 6, line 35-28, col. 9, line 22-45). Surazski is silent on buffering a plurality of cells until every one of the plurality of cells is received.

In a communication system that schedules and manages ATM data, Bonomi discloses a switch environment supporting efficient transmission of frames wherein managing of cell routing is implemented, wherein the architecture includes a plurality of cells being received (cells in frame), and ATM switch buffers all cells of a frame until the last cell of a frame is received, then transmits the whole frame as associated with scheduling (Abstract, col. 5, line 25-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement buffering a plurality of cells until every cell (burst/frame) is received as taught by Bonomi with the teachings of Surazski for the purpose of further managing cell routing, improving transmission speed and increasing throughput.

Allowable Subject Matter

1. Claim 1-32, 37-40, 42, 43-50 and 53-97 is allowed over prior art.
2. The following is a statement of reasons for the indication of allowable subject matter:
Although the prior art discloses routing in a communication system that utilizes arbitration schemes and communicating RTS data, they fail to teach or suggest with respect to claims 1-2, a switch fabric that includes a plurality of fabric gateways and an arbitration component configured to arbitrate a second plurality of RTSs, with respect to claim 3, wherein shifting the frame position for each cell of a column one additional row from a shifted frame position in a prior column, with respect to claim 5, shifted frame associated with a plurality of rows, each row associated with the shifted frame associated with an output link, respect to claims 7-10, reordering the plurality of cells within the frame to produce a shifted frame, each cell being reordered so that each row associated with the frame is uniquely associated with a time slot associated with the shifted frame, with respect to claim 11, time-division de-multiplexing a plurality of CTSs associated with a second frame, a first CTS from the plurality of CTSs associated with a second frame being associated with an availability of a first RTS associated with a cell from the plurality of cells of a first frame, with respect to claim 13, third frame cells being next in time from the plurality of cells associated with the first frame, with respect to claim 14, a cell slot translator configured to shift, with respect to claims 15-22 & 75, switch fabric that includes control portion that is unrelated to data portion of a cell, wherein the control portion includes RTS that identify virtual output queue (VOQ) having a buffered data portion, grouping a first plurality of RTSs and a second plurality of RTSs to produce a set of grouped RTSs, and arbitrating the set of grouped RTSs to produce a plurality of selected RTSs, with respect to claims 23-25, comparators coupled to a second memory wherein the comparators are

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configured to compare an input port schedule value with the plurality of input port requests to produce an output port grant, each comparator from the plurality of comparators being further configured to compare an output port schedule value with a plurality of output port grants including the produced output port grant to produce an input port/output port designation, with respect to claims 26-27, a switch fabric that include grouping a plurality of RTS, forming a plurality of vectors based on the grouped RTSs, wherein each vector is associated with a timeslot representing a status of an output port request for each link, with respect to claims 28-32, RTSs being stored in a grouping memory and the arbitration component arbitrating concurrently the first plurality of RTSs to produce a plurality of selected RTSs, with respect to claims 37-40, data alignment controller configured to send a forwarding signal to the data storage controller at the latest receipt time associated with the plurality of data cells that is within a timeout period, with respect to claim 42, before sending plurality of cells, providing an idle cell for each cell from the plurality of cells that are not received within timeout period, with respect to claims 43-50, a first receipt time and a second data cell associated with the first time slot and a second receipt time later than the first receipt time, with respect to 53-64 and 71-73, a switching fabric that includes a plurality of fabric gateway components coupled to a plurality of multiplexer/de-multiplexer components and providing at least a third plurality of multiplexer/de-multiplexer components coupled to its own plurality of fabric gateway components, removably coupling the first plurality of switching components and the second plurality of switching components to the first plurality of multiplexer/de-multiplexer components, the second plurality of multiplexer/de-multiplexer components, with respect to claim 65, reconfiguring the first plurality of configurable components from the second configuration to the first configuration and removably coupling the second plurality of configurable components to the first plurality of configurable components, with respect to claims 62-64, a switch fabric that includes a plurality

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of fabric gateway components, a first set of configurable components coupled to a plurality of fabric gateway components, with respect to 69, providing at a third plurality of multiplexer/demultiplexer cards coupled to its own plurality of line cards, providing a second plurality of switching cards and removably coupling the first plurality of switching cards and the second plurality of switching cards to the first plurality of switching cards and the second plurality of switching cards to the first, second and third plurality of mux/demux cards, with respect to 74, distributed scheduler having a control path with a rate less than a rate of a control path of a centralized scheduler with a data path having a rate similar to the data rate of the distributed scheduler with respect to claims 76-82, buffering the plurality of cells in a plurality of virtual output queues (VOQ) wherein a first VOQ being associated with the first priority value and the second priority value, each remaining VOQ from the plurality of VOQs being uniquely associated with a remaining priority value from the plurality of priority values, with respect to claim 90, distributed scheduler specifies to a source the destination to which the source should forward data by providing a CTS to the source, with respect to claims 87, a scheduler arranged to receive control information and data from a source within a random time slots, and specify to source at least one destination to which the source should forward further data associated with the control data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prenell P. Jones whose telephone number is 571-272-3180. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prenell P. Jones 

May 17, 2007



CHI PHAM
SUPERVISORY PATENT EXAMINER

5/18/07